

Customer No.: 31561
Application No.: 10/065,750
Docket No.: 8711-US-PA

AMENDMENTS

1. (currently amended) A method for fabricating a nitride read-only memory, comprising:
forming a silicon oxide/silicon nitride/silicon oxide (ONO) stacked layer on a substrate,
the ONO stacked layer consisting of a bottom oxide layer, a silicon nitride layer and a top oxide
layer;
forming a protective layer on the ONO stacked layer, wherein a thickness of the
protective layer is smaller than 50Å;
patterning the protective layer and the ONO stacked layer to form a plurality of stacked
patterns, wherein an etching rate of the protective layer is lower than an etching rate of the top
oxide layer; and
removing the protective layer.
2. (original) The method of claim 1, wherein removing the protective layer comprises
using wet etching to remove the protective layer.
3. (original) The method of claim 1, wherein a thickness of the bottom oxide layer is
about 50~100Å.
4. (original) The method of claim 1, wherein a thickness of the silicon nitride layer is
about 55~80Å.
5. (original) The method of claim 1, wherein a thickness of the top oxide layer is about
70~120Å.

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6. (original) The method of claim 1, the protective layer comprises silicon nitride.

Claim 7: canceled

8. (original) The method of claim 1, further comprising:

performing an ion implantation to form a plurality of buried bit lines in the substrate between the stacked patterns;

forming an insulator on each buried bit line; and

forming a plurality of word lines on the substrate.

9. (original) The method of claim 8, wherein the ONO stacked layer is patterned until a portion of the bottom oxide layer is exposed.

10. (original) The method of claim 9, wherein the exposed bottom oxide layer is removed after the ion implantation is performed.

11. (original) The method of claim 8, wherein the insulator comprises silicon oxide.

12. (original) The method of claim 8, wherein the word lines comprise polysilicon.

13. (original) A method for fabricating a nitride read-only memory, comprising:

forming a silicon oxide/silicon nitride/silicon oxide (ONO) stacked layer on a substrate, the ONO stacked layer consisting of a bottom oxide layer, a silicon nitride layer and a top oxide layer;

forming a protective layer on the ONO stacked layer, the protective layer having a thickness smaller than 50Å;

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patterning the protective layer and the ONO stacked layer to form a plurality of stacked patterns, wherein an etching rate of the protective layer is lower than an etching rate of the top oxide layer;

performing an ion implantation to form a plurality of buried bit lines in the substrate between the stacked patterns;

forming an insulator on each buried bit line; and

forming a plurality of word lines on the substrate.

14. (original) The method of claim 13, wherein a thickness of the bottom oxide layer is about 50~100Å.

15. (original) The method of claim 13, wherein a thickness of the silicon nitride layer is about 55~80Å.

16. (original) The method of claim 13, wherein a thickness of the top oxide layer is about 70~120Å.

17. (original) The method of claim 13, the protective layer comprises silicon nitride.

18. (original) The method of claim 13, the insulator comprises silicon oxide.

19. (original) The method of claim 13, wherein the word lines comprise polysilicon.

20. (original) The method of claim 13, wherein the ONO stacked layer is patterned until a portion of the bottom oxide layer is exposed.

21. (original) The method of claim 20, wherein the exposed bottom oxide layer is removed after the ion implantation is performed.